



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/627,289

07/25/2003

Sean C. Erickson

03-0805

4274

24319

7590

12/28/2004

LSI LOGIC CORPORATION

1621 BARBER LANE

MS: D-106

MILPITAS, CA 95035

EXAMINER

TRINH, HOA B


ART UNIT

PAPER NUMBER

2814

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/627,289	Applicant(s) ERICKSON ET AL.	
	Examiner Vikki H. Trinh	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 18-27 is/are pending in the application.
- 4a) Of the above claim(s) 18-27 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7, 11-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Jin et al. (6,351,039).

Jin et al. '039 discloses a transistor structure having a gate electrode 110 (fig. b) formed of silicided polysilicon (col. 3, lines 5-9), a gate signal 352 (fig. c), and a plurality of conductive plugs 330 (fig. b) made of materials from Group IVB, VB, VIB, and/or VIIB metal (col. 5, lines 57-63), each of the plurality of conductive plugs electrically interconnecting the single gate electrode and the gate signal line (fig. b and fig. c), wherein the gate electrode, plug, and signal line are vertically arranged with respect to the substrate 102 (figs. 3b and 3c).

As to claim 2, the plug has two layers. See fig. 3b.

As to claim 3, each of the two layers is formed of different material (col. 5, lines 57-63).

As to claim 4, 7, the plug has a rectangular cross section. See fig. 3b.

As to claim 11, the plug is formed of tungsten (col. 3, lines 40-41).

As to claim 12, the gate signal line is copper. See fig. 3c.

As to claim 13, the signal line is Al. (col. 3, line 41).

As to claim 14, the gate electrode is shared with other transistor structures. See fig. 3b.

As to claim 15, some of the transistor do not have a conductive plug 330. See fig. 3b.

As to claim 16, the other transistor structures include conductive plugs 130, 330. See fig. 3b and fig. 3c.

As to claim 7, the transistor structure has a second plug 330. See fig. 3b.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

Art Unit: 2814

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 5-6, 8-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al.. Jin et al. '039 discloses the invention substantially as claimed. However, Jin et al. '039 does not explicitly teach the specific dimensions of the width, length, and height/thickness of the plug and gate electrode. Nonetheless, as to claims 5-6, 8-9, it would have been obvious to one skilled in the art at the time the invention was made to construct the invention of Jin et al. with the dimensions as claimed, since it is a prima facie obvious to an artisan for performing optimization and experimentation with the specific dimensions such as the width, length, and height/thickness of the plug and gate because applicants have not yet established any criticality for the specific dimensions.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)

As to claim 10, Jin et al. '039 teaches tungsten of Group VIb from the Periodic Table to make the plug. However, Jin et al. '039 does not explicitly teach chromium or molybdenum of the same Group VIb for the plug. Nonetheless, it would have been to one skilled in the art at the time the invention was made to select a different material compound in the same Group VIb for the plug, since it is a prima facie obvious to an artisan in selecting different material of the same Group for use in optimizing or experimenting with the transistor structure.

Response to Arguments

8. Applicant's arguments filed October 07, 2004, have been fully considered but they are not persuasive.

In the remarks, applicant contends that Jin does not disclose every elements of claim 1. In particular, applicant argues that the newly amended claim 1 includes a plurality of conductive plugs electrically interconnecting the single gate electrode and the gate signal line, which Jin lacks. On the contrary, Jin does disclose and teach every limitations of claim 1 in the present application. As stated in the rejection above, Jin shows a transistor structure having a gate electrode 110 (fig. b) formed of silicided polysilicon (col. 3, lines 5-9), a gate signal 352 (fig. c), and a plurality of conductive plugs 330 (fig. b) made of materials from Group IVB, VB, VIB, and/or VIIB metal (col. 5, lines 57-63), each of the plurality of conductive plugs electrically interconnecting the single gate electrode and the gate signal line (fig. b and fig. c), wherein the gate electrode, plug, and signal line are vertically arranged with respect to the substrate 102 (figs. 3b and 3c). Moreover, applicant fails to claim the limitations of claim 1 of the present application, so that the language of the claim 1 is consistent with applicant's argument. (For example, applicant claims in claim 1, line 5, "**each** of the plurality of conductive plugs electrically interconnecting the single gate electrode and the gate signal line..". This phrase means each plug electrically interconnecting a gate electrode and a gate signal line. Contrary to applicant's argument, the phrase does not mean the same as applicant stated in the remarks, "the plurality of conductive plugs electrically interconnecting the single gate electrode and gate signal line"). Furthermore, applicant misconstrues the examiner's rejection by directing to the previous Office Action to fig. 3a and fig. 3b (Applicant's remarks, page 8, line 8), when the examiner

applies fig. 3b and fig. 3c of Jin to claim 1 of the present application. Nonetheless, Jin discloses all of the limitations of claims 1-4, 7, and 11-13. Therefore, the rejection is maintained.

As to claims 5-6 and 8-10, applicant argues that the rejection is traverse because the claims depend on claim 1 which is believed to be allowable. The examiner notes that applicant's argument is not persuasive because claim 1 is a rejected claim.

For the foregoing reasons, the examiner maintains the rejection of the previous Office Action.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If

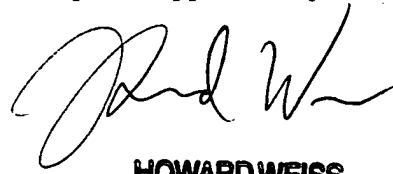
Art Unit: 2814

attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,
Patent Examiner
AU 2814



HOWARD WEISS
PRIMARY EXAMINER